Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) A method of processing a data signal, comprising:

receiving a differential data signal;

determining if said differential data signal represents a valid data word from a plurality of valid data words; and

if said differential data signal does not represent a valid data word from said plurality of valid data words, then inverting said differential data signal, producing an inverted differential data signal, and determining if said inverted differential data signal represents a valid data word from said plurality of data words.

2. (Currently Amended) The method of claim 1, wherein said step of inverting includes the step of X-ORing said [[data]] differential data signal with a control bit, said control bit being a logic "1" if said differential data signal represents an invalid data word.

3. (Original) The method of claim 2, wherein said control bit is a logic "0" if said differential data signal represents a valid data word.

4. (Original) The method of claim 1, further comprising the step of further processing said inverted differential data signal.

5. (Original) The method of claim 1, further comprising the step of serializing said inverted differential data signal.

6. (Original) The method of claim 5, further comprising the step of transmitting the result of said serializing step to a destination node.

7. (Original) The method of claim 1, wherein said step of determining comprises the step of comparing a data word represented by said differential data signal with one or more valid data words stored in a memory.

8. (Original) The method of claim 7, further comprising the step of generating a control signal based on said step of comparing.

9. (Original) The method of claim 7, wherein said control signal represents a logic "1" if said data word represented by said differential data signal is not consistent with at least one of said valid data words, and wherein said control signal represents a logic "0" if said data word is consistent with at least one of said one or more valid data words.

10. (Original) The method of claim 1, further comprising the step of determining if said inverted differential data signal represents a valid data word.

11. (Original) The method of claim 10, further comprising the step of further processing said inverted differential data signal if said inverted differential data signal represents a valid data word.

12. (Original) The method of claim 1, wherein said differential data signal includes a first component and a second component, and wherein said step of inverting comprises the step of inverting a logic state of said first component of said differential data signal, and inverting a logic state of said second component of said differential data signal.

13. (Currently Amended) A method of processing a data signal, comprising:

receiving a differential data signal having a first component and a second component;

comparing a data word represented by said differential data signal with one or more valid data words;

if said data word of said differential data signal is not consistent with at least one of said one or more valid data words, then inverting said first component and said second

component of said differential data signal, producing an inverted differential data signal, and determining if said inverted differential data signal represents the valid data word.

14. (Original) The method of claim 13, further comprising the steps of:

generating a control signal if said data word of said differential data signal is not consistent with at least one of said one or more valid data words, said control signal having a logic state "1"; and

X-ORing said control signal with said first and second components of said differential data signal to produce said inverted differential data signal.

15. (Currently Amended) A transceiver, comprising:

a receiver input for receiving a serial data signal;

a serial-to-parallel converter coupled to an output of said receiver input;

an error check for determining if a differential output of said serial-to-parallel converter represents a valid data word from a plurality of valid data words; and

a logic circuit for inverting said differential output if said differential output does not represent a valid data word to produce an inverted differential output, wherein said error check model further determines if said inverted differential output is a valid data word from said plurality of valid data words.

16. (Original) The transceiver of claim 15, wherein said logic circuit includes a X-OR circuit having said differential output as a first input and a control signal as a second input.

17. (Original) The transceiver of claim 16, wherein said control signal causes said X-OR circuit to invert said differential output of said serial-to-parallel converter if said differential output does not represent a valid data word.

18. (Original) The transceiver of claim 17, wherein said control signal is a logic "1" if said differential output does not represent a valid data word, and said control signal is a logic "0" if said differential output represents a valid data word.

19. (Original) The transceiver of claim 17, wherein said error check includes a memory that stores one or more valid data words, and wherein said error check generates said control signal based on a comparison between said differential output and said one or more valid code words.

20. (Original) The transceiver of claim 19, wherein said error check generates said control signal to have a logic "1" if said differential output is not consistent with at least one of said valid code words.

21- 23. (Canceled)